REMARKS

This is in response to the Office Action mailed on February 12, 2004, and the references cited therewith. Claims 1, 2, 7, 12 and 21 are amended, claims 8-11 are canceled, and claims 23-26 are added; as a result, claims 1-7 and 12-26 are now pending in this application.

§101 Rejection of the Claims

Claims 8-11 were rejected under 35 USC § 101 as being directed to non-statutory subject matter. Claims 8-11 have been canceled.

§102 Rejection of the Claims

Claims 1-22 were rejected under 35 USC § 102(b) as being anticipated by Faanes et al. (US 6,496,902).

Faanes describes a cache structure that can be used in the processors of a computer system having a main memory and two or more processors connected to the main memory. Faanes notes the difficulty in invalidating the cache when, for instance, swapping tasks in the computer. He notes that "a conventional cache invalidates approximately one line of data (i.e., about 8 words or 64 bytes) per clock cycle." *Faanes*, col. 12, lines 32-34.

Faanes notes that cache invalidation is typically performed when swapping tasks in the computer. In order to speed cache invalidation at these times, Faanes describes a cache structure which "invalidates large amounts of data in a relatively few clock cycles (e.g., 256 K bytes in approximately 6 to 8 clock cycles)." To do this, Faanes teaches running an invalidate-cache signal from processor 110 to each cache chip 120. The invalidate-cache signal "is activatable by a program instruction (e.g., a "test-and-set" instruction) and/or task-swap function." *Faanes*, col. 12, lines 30-40.

In contrast, Applicant teaches that resource synchronization instructions can be used to synchronize processors all trying to access the same resource. Such instructions can be made even more advantageous if they are enhanced to invalidate some or all of the cache local to the processor at the same time that they are accessing one or more locations in main memory. Applicant notes that, for some legacy programs, it is best, however, to be able to disable this function. Applicant has amended claims 1, 2, 7, 12 and 21 to accentuate these differences over

Faanes and the other cited references and has added new claims 23-26 to claim a computer having such an instruction set.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date July 12, 2004

By Thomas F. Brennan
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 12th day of July, 2004.

CANDIS BUENDING

Name

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